A NEW METHOD TO CALCULATE PARAMETERS OF CONFIGURABLE INTEGRATED TEST MODEL*

Huei Wang, Daniel Yang, Gary Ng and Sian-Tek Chen

TRW
Microwave Technology Development Operation
One Space Park, Redondo Beach, CA 90278

ABSTRACT

A configurable integrated test (CIT) model has been developed for GaAs MMIC manufacturing control. The optimal process/test strategy of a MMIC in production phase can be predicted from this model. A new method using optimization concept is demonstrated to calculate parameters of the CIT model from process/test history. This method will estimate realistic screening probabilities and hence predict optimal test strategy accurately. The description of this new method and examples are presented in this paper.

CONFIGURABLE INTEGRATED TEST MODEL

It is well known that the cost of test dominates the MMIC manufacturing cost [1]. The establishment of a test plan is then a very important task before the production of a specific chip. A systematic method, called configurable integrated test (CIT) [2-3], has been developed to analyze the detailed yield and cost effects in production and predict the optimum test strategy (in terms of cost). This concept is implemented into a mathematical model based on the characterization of each process and/or test step during manufacturing. Engineers can use this model to simulate the yield and cost of all the possible combinations and sequences of test procedures. As a consequence, the optimal process/test strategy can be predicted. Quantitative prediction of all potential test strategies with the CIT model results in an accurate cost estimation for the mass production of chips. It is noted that for some cases the cost of a MMIC chip could be reduced by up to 50% according to the "what if" scenarios suggested by the CIT model. This number can be even higher if some high efficiency and low risk test technology is developed and used.

The CIT model in a MMIC chip production is characterized by a series of process/test steps including in-process tests, on-wafer tests and chip tests. Each step contains three screening probabilities: screening **efficiency** (chance of identifying and rejecting a bad unit, denoted as e), screening **risk** (chance of misidentifying and rejecting a good unit, r) and **fallout** (chance of degrading a good unit to a bad one during test/process, f). A "potentially good" (or simply "good") unit means the unit will meet final specifications if not degraded in later process or test steps. A "bad" unit at a certain step is a unit which is not potentially good. The cost functions associated with each step consist of fixed cost (c_f) and unit cost (c_u). The quantities to be calculated from the model are defined as input and output (I/O) functions of each step, and include yield (Y), the number of total remaining units (N), the percentage of potentially good units (G) and cumulated unit cost (C).

A block diagram in Fig. 1 illustrates I/O functions and model parameters of each step. The subscript i stands for each quantity of step i. The input of step i is simply the output of step $i-1$. These I/O functions for a MMIC with M process/test steps are described by a set of recursive equations which related with model parameters as

$$N_i = N_{i-1} Y_i \tag{1}$$

$$Y_i = 1 - e_i + (e_i - r_i) G_{i-1} \tag{2}$$

$$G_i = (1 - r_i - f_i) \frac{G_{i-1}}{Y_i} \quad , \tag{3}$$

*This work is support by the MIMIC Phase 1 Program (Contract DAAL01-88-C-0835) sponsored by the Electronics Technology & Device Laboratory of U. S. Army.

$$C_i = C_0 + \sum_{k=1}^{i} (c_{fk} + c_{uk} N_{k-1}) , \qquad (4)$$

for $i = 1, 2, ..., M$. The initial conditions from the wafer initiation are also needed for the recursive calculation of outputs of each step:

N_0 = initial unit number,

G_0 = percentage of potentially good unit before wafer process,

C_0 = cost of wafer initiation.

The recursive relations (1) to (4) essentially form a system of difference equations, and the I/O functions are simply state variables from a system's point of view. The derivations of equations (1) to (4) are based on the definitions of I/O functions and model parameters, where (2) and (3) can be carried out by using the relative occurrence frequency interpretation of probability without much difficulties. Equations (1) and (4) are simply the definitions of the yield for a single step and the cumulated cost. For detailed description of this model, see [2].

NEW METHOD TO DETERMINE MODEL PARAMETERS

Since cost functions of each process/test step in the CIT model are dependent of process recipes and test techniques, this issue is not discussed here. For the screen probabilities, there are several ways to determine them as presented in [2] and [4]. However the method using complete process/test yield history mentioned in [2] is most straightforward and intuitive. It is briefly described here.

Let us define the following sets during a particular step i:

F = the collection of units rejected at step i,

G = the collection of potentially bad units before step i,

H = the collection of potentially good units before step i,

E = the collection of good units degraded to bad ones during step i.

Then the three screen probabilities can be expressed as

$$e_i = P(\mathbf{F}|\mathbf{G}), \quad r_i = P(\mathbf{F}|\mathbf{H}), \quad f_i = P(\mathbf{E}|\mathbf{H}) \qquad (5)$$

and can be calculated from the definition of of conditional probability of event **X** given event **Y**:

$$P(\mathbf{X}|\mathbf{Y}) = \frac{P(\mathbf{X} \cap \mathbf{Y})}{P(\mathbf{Y})} = \frac{N_{\mathbf{X} \cap \mathbf{Y}}}{N_{\mathbf{Y}}} , \qquad (6)$$

where $N_{\mathbf{X}}$ stands for the number of elements in a finite set **X**.

The new method is presented as follows. For a complete process/test history of a particular MMIC chip, the parameters of the ith step e_i, r_i and f_i $(1 < i < M)$ can be estimated from (5) and (6) for a certain test sequence. Since the adaptive or "configurable" nature of this CIT model is based on the assumption that for each individual MMIC, the model parameters of step i are invariant for given final specifications and the ith screen criteria under the same test conditions, in reality the model parameters will not be identical in general if some of the previous screen criteria are changed. In order to overcome this inconsistency, the concept of least error solution for an over-determined system of linear algebra equations can be applied to resolve this issue and thus estimate the more realistic parameters.

Suppose there are n realistic and non-trivial modifications of screening criteria of the testing procedure before the ith step. A non-trivial modification of screening criteria simply means that the quantities Y_i, G_i and G_{i-1} obtained from the test history with modified criteria are different form those with other criteria. However under these n different situations the test conditions remain the same at step i, that means e_i, r_i and f_i can be assumed to be the same for these n

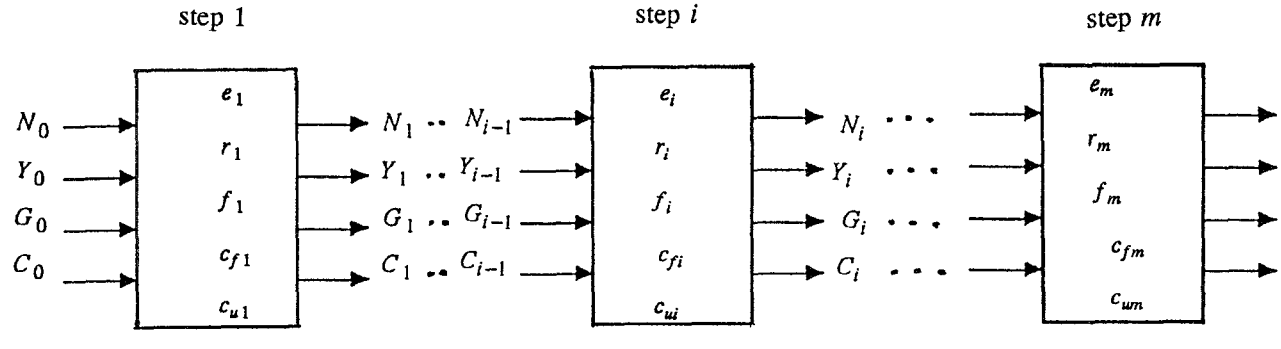

Fig. 1. Block diagram of CIT model.

situations.

Now the invariant parameters e_i, r_i and f_i can be determined. Since there are n sets of Y_i, G_i and G_{i-1} from n non-trivial modifications of screening criteria, denoted as Y_i^j, G_i^j and G_{i-1}^j for $j = 1,..., n$, we can apply these quantities to equations (2) and (3), then there will be $2n$ equations for 3 unknowns (e_i, r_i and f_i):

$$\begin{aligned} Y_i^1 &= 1 - e_i + (e_i - r_i)G_{i-1}^1 \\ G_i^1 &= (1 - r_i - f_i)\frac{G_{i-1}^1}{Y_i^1} \\ &\cdots\cdots\cdots\cdots \\ &\cdots\cdots\cdots\cdots \\ Y_i^n &= 1 - e_i + (e_i - r_i)G_{i-1}^n \\ G_i^n &= (1 - r_i - f_i)\frac{G_{i-1}^n}{Y_i^n} \end{aligned} \qquad (7)$$

These $2n$ equations form an over-determined system of linear algebra equations. The least error solutions of (7) can be obtained as the optimal parameters for certain choices of norm. Since the screening probabilities are all bounded by 0 and 1 according to the definition of probability, this problem can also be classified as a constrained optimization problem. The same approach applies to other steps except the first one.

EXAMPLES

A set of CIT model parameters has been derived from the new method for a monolithic MESFET two stage IF amplifier currently fabricated under GaAs MANTECH Program*. This amplifier occupies a chip size of 84×46 mil^2 and utilizes feedback at the first stage [5]. The predicted gain is 15±1 dB from 1.5 to 4.5 GHz, and the input and output VSWR less than 2.0 over the frequency band. More than fifteen thousand (15,000) chips have been tested during production. The manufacturing process and test procedure of this amplifier are characterized into fourteen (14) steps, as depicted in Fig. 2. There are six in process tests (IPT) including steps 1 to 6 for wafer process monitoring in the top side processing phase, each IPT is performed after a certain process as specified in the figure. Steps 7 to 11 are on-wafer DC and RF functional test along the tail end process (backside metal process, wafer dice and chip assemble). Steps 12 to 14 are the final assurance tests.

Our CIT model can be applied to this chip manufacture for illustrating the significance of this new test strategy. For the first example, four different test strategies with combinations of on-wafer DC and RF circuit functional test (steps 7 and 9) are simulated. The results of cumulated unit cost versus four different test strategies are shown in Fig. 3. All the cost numbers are normalized to the highest cost option. One can observe that the lowest cost procedure is the one performing RF test but skipping DC test, which reduces the chip unit cost by 26% if compared with the option which skipping both DC and RF tests. The second example is a high reliability (Hi-Rel) application, for which the chip assembly cost is twelve times higher than the previous example. The importance of on-wafer RF circuit functional test is much more significant since the high chip assembly cost can be greatly saved if bad units are screened out early. The cost reduction becomes 42% by the comparison of the option with both DC and RF tests between the one skipping both DC and RF tests (Fig. 4).

	MMIC Process/Test
seq	step
0	lot initiation
1	IPT1 (implant & anneal)
2	IPT2 (ohmic contact)
3	IPT3 (TFR)
4	IPT4 (gate recess)
5	IPT5 (gate metal)
6	IPT6 (top metal);TEG
7	DC functional test
8	back side process
9	RF functional test
10	dice and select
11	assemble (carrier)
12	pretest
13	burn in
14	acceptance test

Fig. 2. Fourteen steps of process/test procedure of the MESFET MMIC.

CONCLUSION

The optimization (least error) concept has been applied to determine the parameters for the CIT model which is developed for systematic analysis of process/test strategy. Significant cost reduction can be achieved by using this tool to predict the optimal test strategy with accurate model parameters. This CIT model can provide

*Manufacturing Technology Program for solid state system is supported by Directorate of Wright Research and Development Center at Write-Patterson AFB under Contract F33615-85-C-5604 to Westinghouse Corporation.

real-time test evaluation and feedback to engineers if integrated with test data base. It is believed that the CIT model will play a very important role in managing and controlling GaAs MMIC chip manufacturing cost in the near future.

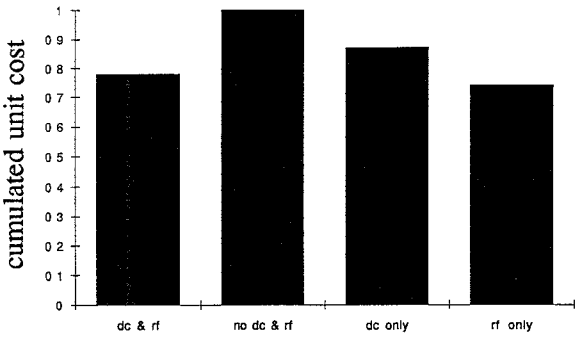

Fig. 3. Simulation results for four different test strategies.

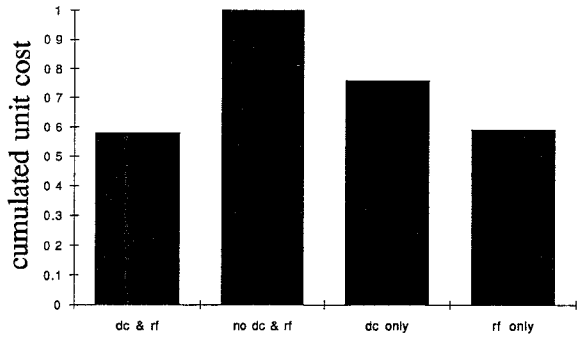

Fig. 4. Simulation results for Hi-Rel application.

ACKNOWLEDGMENT

The authors would like to thank Dr. Louis C. T. Liu, Dr. R. Esfandiari and Dr. T. Joseph for their helpful discussions and suggestions. The authors would also like to thank MANTECH Program for the supply of MMIC test data.

REFERENCES

[1] Frank A. Brand, "1988 IEEE MTT-S International Microwave Symposium Keynote Address," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1567-1577, Dec., 1988.

[2] H. Wang, D. Yang, R. Esfandiari, T. Joseph and G. Ng, "Application of Configurable Integrated Test for MMIC Production Control," *11th Annual IEEE GaAs IC Symposium Digest,* pp. 227-230, Oct., 1989.

[3] Arvind K. Sharma, Robert K. Ellis, Jeffrey P. Kenyon, Louis C. T. Liu and Marshall Y. Huang, "Reduce MMIC Production Costs Using Integrated Testing and Modeling System," *MSN,* pp. 55-62, July, 1989.

[4] C. T. Matsuno, Arvind K. Sharma, H. Wang, D. C. Yang, "Adaptive Control of MMIC Module Production Costs," *Government Microcircuit Applications Conference (GOMAC) Digest,* pp. 69-72, Nov., 1989.

[5] D. C. Yang, R. Esfandiari, T. S. Lin and T. J. O'Neill, "Wideband GaAs MMIC Receiver," *IEEE Monolithic Circuit Symposium Digest,* pp. 101-104, June, 1987.